REMARKS

In the Office Action mailed on August 26, 2004, claims 1-21 are rejected under 35 USC §103(a) as being unpatentable over the combination of Jones et al. (U.S. Patent 6,356,960, "Jones") and Rieken (U.S. Patent 6,665,817). Claims 22 and 23 are considered allowable subject matter if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In response to the rejection of the claims as being unpatentable over the combination of Jones and Rieken, Applicant has amended each of the independent claims 1, 7 and 13 to include:

(i) that the user-specified event of the breakpoint unit can be programmed through a debug port,

(ii) stopping the system clock such that the state of the programmable hardware is held static, and

(iii) accessing the static state of the programmable hardware through the debug port.

Applicant respectfully submits that none of these elements is found in either of the references.

It is stated in the Office Action that Jones fails to teach a break point unit connected to the internal bus system, such that the breakpoint unit can be programmed through a debug port. Rieken is cited for teaching a breakpoint unit connected to an internal system bus and capable of being programmed through a debug port, specifically in Fig. 5 and col. 4, line 50 to col. 5 lines 1-25. However, Applicant's invention is directed to a method and apparatus for diagnosing programmable hardware. Each independent claim as amended specifically recites accessing the static state of the programmable hardware through the debug port. In addition to failing to disclose or suggest enabling the user-specified event to be programmed through the debug port, neither reference discloses nor suggests accessing the static state of the programmable hardware through the deport bug.

Referring specifically to the primary reference, Jones is related to a computer system including a microprocessor on an integrated circuit chip having an on-chip CPU. A communication bus provides a parallel communication path between the CPU

and a local memory. Although the integrated circuit device further comprises a debugging port connected between the bus on the integrated circuit chip and an external debugging computer device (i.e. external host), the only reference to programmable hardware in Jones is the suggestion that the "external host may comprise a computer or a computer device such as a programmable logic array." (Col. 15, lines 36-37). Accordingly, Jones also fails to disclose or suggest "stopping the system clock such that the state of the programmable hardware is held static," or "accessing the static state of the programmable hardware through the debug port."

Similarly, while the system of Reiken uses programmable logic, Reiken also fails to disclose or suggest the steps of diagnosing programmable hardware. In contrast to Applicant's invention, Reiken discloses using programmable hardware to enable a diagnostic tool of an integrated circuit. Reiken relates to a wireless communication system-on-a-chip comprising a system bus, and a set of fixed function processors, an embedded processor, and reconfigurable logic, each connected to the system bus. The reconfigurable logic supports an operational mode and a diagnostic mode. In the operational mode, the system operates to support different air interface protocols and data rates. In the diagnostic mode, the system alternately tests the system, debugs the system, and monitors bus activity within the system. (Col. 1, lines 51-60).

While Reiken discloses using programmable logic as a diagnostic tool, Reiken fails to disclose or suggest a tool for diagnosing programmable logic. In particular, Fig. 5 discloses a DBG_IF block 118 which is embedded in a core 120 and establishes interface logic associated with the embedded processor core to support the debugging functions to the core. A DBG_CNTL block 122, which is included in the reprogrammable logic 114, is a controller which allows the external JTAG interface to control and observe the registers contained in the RL debugger logic. This allows the breakpoint registers to be setup, bus or control signals to be monitored and serially scanned out, and the scanning in of new instructions. Blocks BLO 124 and BL1 126 in the reprogrammable logic 114 operate as breakpoint units which compare data/address/control values "from the bus and core to determine when a breakpoint has occurred." Upon completion of any temporal debugging functions, the

reprogrammable logic 114 is then configured for its final, resident application. (Col. 5 lines 9-25).

Therefore, the architecture of Reiken minimizes the dedicated hardware for runtime debugging support in an embedded processor, and provides post-manufacturing configurability of debugging resources. (Col. 5, lines 28-32). However, in addition to failing to disclose or suggest that the user-specified event of the breakpoint unit can be programmed through a debug port, Reiken fails to disclose or suggest stopping the system clock such that the programmable hardware is held static, or accessing the static state of the programmable hardware through a debug port. Accordingly, any combination of Jones and Reiken would not lead to Applicant's invention as claimed. Applicant further submits that dependent claims 2-6, 8-12 and 14-23 are allowable for at least the same reason that the independent claims are believed allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the Applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on November 23, 2004.

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AMENDMENTS TO THE DRAWINGS

The drawings are objected to under 37 CFR §1.83(a) for failing to show every feature of the invention specified in the claims. Applicant has amended Fig. 1 to shown a bus, in addition to the CSI bus, and therefore create a plurality of buses. Applicant attaches a marked-up copy of Fig. 1 showing the additional bus. Applicant submits that no new matter is raised by the amendment to Fig. 1. Support for the amendment can be found at least on page 5, lines 4-7 of Applicant's specification. A complete set of formal drawings is also attached.